<u>AMENDMENTS TO THE CLAIMS</u>:

Please amend the claims as follows:

1-4. (Cancelled)

5. (Currently amended) A method for manufacturing a semiconductor device, comprising the steps of:

forming an amorphous layer in a region from a surface of a semiconductor region of a first conductivity type to a first depth;

by heat treating the amorphous layer at a prescribed temperature ~~without implanting ions into the amorphous layer~~, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth;

after the heat treating, forming a first impurity layer of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions into the ~~heat-treated~~ amorphous layer <u>extending from the surface of the semiconductor region to the second depth</u>; and

~~activating the first impurity layer~~

<u>restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy</u>.

6. (Original) The manufacturing method of a semiconductor device according to claim 5, wherein the third depth is in a range of 5 nm to 15 nm.

7. (Currently amended) The manufacturing method of a semiconductor device according to claim 5, wherein the prescribed temperature is in a range of 475°C to 600°C~~, and the activation of the first impurity layer is conducted in a temperature range of 500°C to 700°C~~.

8. (Cancelled)

9. (Currently amended) A method for manufacturing a semiconductor device, comprising the steps of:

forming a gate electrode on a semiconductor region of a first conductivity type <u>with a gate insulating film interposed therebetween</u>;

forming an amorphous layer in a region from a surface of the semiconductor region ~~of the first conductivity type~~ to a first depth;

by heat treating the amorphous layer at a prescribed temperature ~~without implanting ions into the amorphous layer~~, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth;

after the heat treating, forming a first impurity layer of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions into the ~~heat-treated~~ amorphous layer <u>extending from the surface of the semiconductor region to the second depth</u>;

after the heat treating, forming a second impurity layer of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions into the heat-treated amorphous layer; and

~~activating the first impurity layer and the second impurity layer~~

restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy.

10. (Original) The manufacturing method of a semiconductor device according to claim 9, wherein the third depth is in a range of 5 nm to 15 nm.

11. (Currently amended) The manufacturing method of a semiconductor device according to claim 9, wherein the prescribed temperature is in a range of 475°C to 600°C~~, and the activation of the first impurity layer and the second impurity layer is conducted in a temperature range of 500°C to 700°C~~.

12. (Original) The manufacturing method of a semiconductor device according to claim 9, wherein a pattern of a gate electrode that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region.

13. (Currently amended) A method for manufacturing a semiconductor device, comprising the steps of:

forming a gate electrode on a semiconductor region of a first conductivity type with a gate insulating film interposed therebetween;

forming an amorphous layer in a region from a surface of the semiconductor region to a first depth;

forming an insulating sidewall on a side surface of the gate electrode while restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth, the restoration of the crystal structure of the amorphous layer being caused by heat treatment of a

prescribed temperature which is conducted during formation of the sidewall ~~without implanting ions into the amorphous layer~~;

after the heat treating, forming a first impurity layer of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions on both sides of the gate electrode in the ~~heat-treated~~ amorphous layer <u>extending from the surface of the semiconductor region to the second depth</u>; and

~~activating the first impurity layer~~

<u>restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy</u>.

14. (Currently amended) The manufacturing method of a semiconductor device according to claim 13, further comprising the step of:

after the step of forming the first impurity layer, forming a second impurity layer of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer~~, wherein~~

~~the second impurity layer is simultaneously activated in the step of activating the first impurity layer~~.

15. (Original) The manufacturing method of a semiconductor device according to claim 13, wherein the first impurity layer has a depth of 5 nm to 15 nm.

16. (Currently amended) The manufacturing method of a semiconductor device according to claim 13, wherein the prescribed temperature is in a range of 475°C to 600°C~~, and the activation is conducted in a temperature range of 500°C to 700°C~~.

17. (Original) The manufacturing method of a semiconductor device according to claim 13, wherein a pattern of a gate electrode that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region.

18. (New) The manufacturing method of a semiconductor device according to claim 5, wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 800 °C.

19. (New) The manufacturing method of a semiconductor device according to claim 5, wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 700 °C.

20. (New) The manufacturing method of a semiconductor device according to claim 5, wherein the first impurity layer is activated in the step of restoring the crystal structure using solid phase epitaxy.

21. (New) The manufacturing method of a semiconductor device according to claim 9, wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 800 °C.

22. (New) The manufacturing method of a semiconductor device according to claim 9, wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 700 °C.

23. (New) The manufacturing method of a semiconductor device according to claim 9, wherein the first impurity layer is activated in the step of restoring the crystal structure using solid phase epitaxy.

24. (New) The manufacturing method of a semiconductor device according to claim 13, wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 800 °C.

25. (New) The manufacturing method of a semiconductor device according to claim 13, wherein the first impurity layer is activated in the step of restoring the crystal structure using solid phase epitaxy.